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Design considerations for Radiation Hardened ASIC used as tecnological payload in NANOSATC-BR1

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ABSTRACT

Integrated Circuits (IC) developed for space application requires special care during design, manufacturing and qualification process as they will work on a harsh radioactive environment. There are specially three important kind of interactions which can happen between silicon and radiation: a cumulative long term ionization damage denominated Total Ionization Dose (TID), instantaneous radiation dose effects denominated Single Event Effects (SEE) and Displacement Damage (DD) on crystalline structure of silicon. Due technological restrictions and low production–low demand of space ICs, Radiation Hardening by Design Techniques (RHBD) using conventional

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Complementary Metal-Oxide-Semiconductor CMOS process are become more attractive during the last years. This solution relies on new design techniques, which mitigate the effects of radiation aforementioned. In this paper is shown design techniques and considerations using in the Application Specific Integrated Circuit (ASIC) developed in Santa Maria Design House (SMDH). This ASIC was included as technological payload in the NANOSATC-BR1. The design approaches proposed in this work will be confirmed by results collected during several months. The radiation hardened digital cells designed by SMDH proved a tolerance to solar energetic particles with energies of up to 100MeV.

INTRODUCTION

The mission NANOSATC-BR1 is part of the NANOSATC-BR program. In this mission was developed the NCBR1, a CubeSat (1 U) nanosatellite class, financed by INPE – PNAE.

The NCBR1 was designed with the purpose of performing scientific and technological experiments. The scientific experiment collected data through a magnetometer (XEN-1210 model, with resolution 15nT) to measure the intensity of the Earth Magnetic Field. The technological experiment collected data of the faults caused by instantaneous radiation dose effects (SEE) to test, evaluate and demonstrate in a space environment the radiation tolerant technology used in the ASIC designed by SMDH and in the codes running in the FPGA and synthesized by UFRGS.

The NCBR1 was launched from the Russian Yasny Launch Base by a DNPER launch vehicle on June 19, 2014 and operated in Low Earth Orbit (LEO) that passes through the South Atlantic Magnetic Anomaly. This orbit is an ideal environment for demonstrating the Earth Magnetic Field intensity measurements and integrated circuits (ICs) SEE mitigation strategies. The orbit provides a sufficient amount of time for the system to experience a reasonable number of faults to evaluate the system's radiation tolerance. In this space environment the radiation is mixed, the particle fluence and energy changes due to space weather, the temperature varies, and electromagnetic spectrum fluctuates [1]. The way to assess the real performance of the ICs was to fly in the relevant environment of space.

This paper will describe the ASIC RH-DRVTestChip1 (TC1) that was designed by SMDH.

MOTIVATION

The needs of both science and engineering calls for innovation. The technology relevance here are in incorporating fault-tolerant technologies to increase the robustness of space computing platforms, to enable missions in harsh radiation environments and longer term missions. Currently, typical cubesat missions are short duration and friendly orbits, and cubesat missions with longer duration and harsher orbits are expected in future. Additionally, the prevalence of computer systems in future missions is also expected.

The radiation effects on space computers are caused by ionizing radiation striking the IC substrate and depositing unwanted energy. They are categorized in TID and SEE. The TID causes a gradual degradation and can destroy the device while the SEE causes an instantaneous failure and do not cause permanent damage to the device, but unwanted logic level transitions [2].

To mitigate TID, there are techniques like non-standard layout techniques, also known as radiation-hardened-by-design (RHBD) techniques, like non-standard materials, also known as radiation-hardened-by-process (RHBP) techniques, and like the use of shielding. To mitigate SEE, the mitigation strategies are the redundancy and the memory scrubbing.

TC1 SMDH ASIC

The TC1 has the purpose of demonstrate the radiation tolerant technology in a space environment with statistically significant faults to verify reliable operation and evaluate its SEE immunity in a flight demonstration in space.

Space testing is required because the energy levels necessary to empirically test the system's SEE immunity cannot be produced on earth. Cyclotrons and particle accelerators cannot reproduce the space environment accurately and do not meet the requirements of a full system prototype demonstration in an operational environment [2].

A typical scenario for radiation hardened ICs (like the ones whose design will be enabled by rad-hard library cells) are space applications. In the space applications context, space satellites play a very important role, being a key component on several of such type of application.

Space satellites are composed by platform and payload. The platform, in turn, is composed by basic items such as structure, power, onboard computer, etc. which support payloads operation. Furthermore, the platform is also responsible for monitoring, operation and maintenance of the orbiting satellite, as well as for the communication with ground stations. The payload, on the other hand, is application oriented or, in other words, is the reason why the satellite has been launched. In a remote sensing satellite, for instance, payload is composed by cameras and other sensors.

Once in orbit, satellites need to be monitored and controlled in order to perform the tasks they have been designed for. Satellite monitoring, control and communication are performed through telemetry and telecommand systems. The telemetry system is designed to acquire and format information provided by sensors, transmitting it in a safe way afterwards. The telecomand system, on the other hand, is designed to receive, validate and transmit telecomands comming from ground stations to the respective destination point (inside the satellite). Such commands can be used, for instance, to turn equipments on or off, change subsystem operation modes, load new operation parameters, etc. When sending a command to its respective destination point, specific and standardized interfaces shall be used.

In this way, the TC1 was designed using the SMDH rad-hard library cells with RHBD techniques as radiation mitigation approach. Architecturally, the TC1 consists in a pulse generator used for an on/off type command, a block of shift registers and a set of transistors.

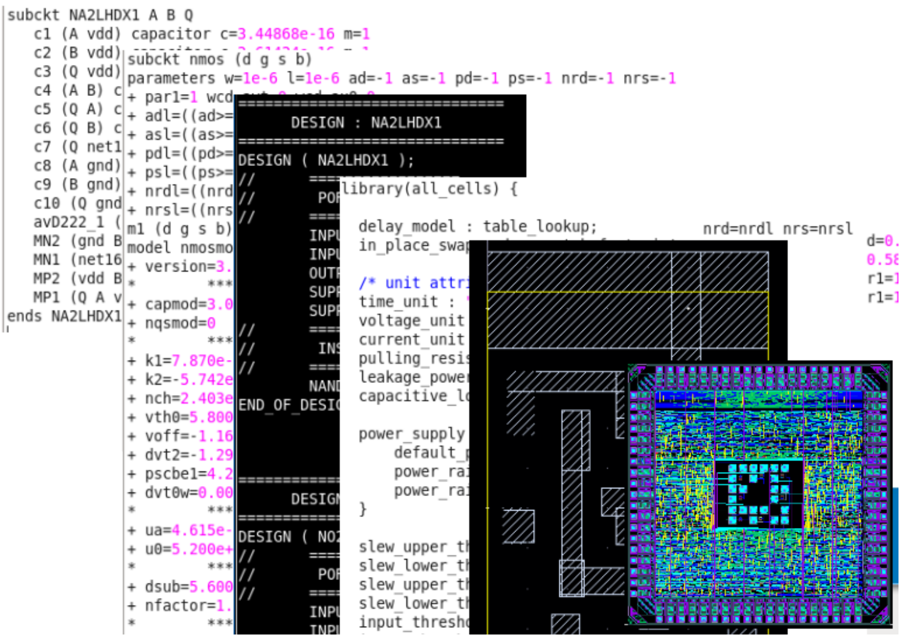

Fig. 1. From SMDH rad-hard library cells to the TC1 ASIC.

The circuit was designed with the intention of performing functional tests during ionizing irradiation in the Low Earth Orbit (LEO). It is controlled by the SMDH Control Block, responsible by generating the stimulus, capturing and storing the responses.

The main objectives of the TC1 are:

- Begin the functional validation of cell library created to enable the design of radiation tolerant circuits, where the on-off driver will be the first of these circuits to be designed;

- Obtain through radiation test in earth the first results of the cell library tolerance to the effects of ionizing radiation, more precisely the TID and SEE effects.

The TC1 consists of:

- Pulse Generator: Digital block that controls the pulses generation for activation/deactivation of secondary circuits as relays. This circuit follow the technical specifications of a Low Voltage-High Power Command (LV-HPC) defined in the Space Discrete Interface Document [3]. Built from a set of the radiation hardened library cells designed by SMDH, it contains the digital portion of the on-off driver (2x4 mux, counter, reset logic). This circuit has dedicated pins for the com SMDH Control. It could be evaluated in relation to the TID, as the SEE.

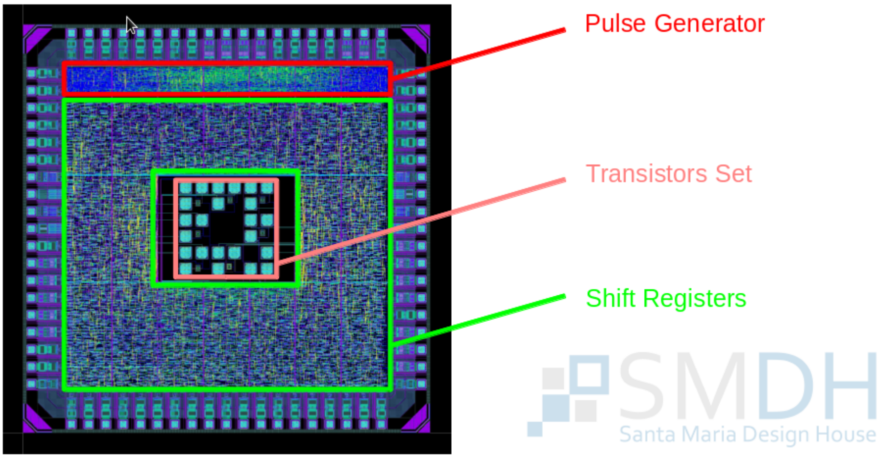

Fig. 2. TC1 Layout.

- Shift Registers: This block is composed of 10 shift registers circuits with different configurations. Shift register is a circuit formed by a sequential chain of registers (flip-flops): the output of a register is connected to the input of the next and so on. There are two sub-groups: the half are shift registers designed with standard cells, and the other half are shift registers designed with rad-hard cells. There is a dedicated set of pins to interface with these two groups of sub-circuits. The shift registers have two different lengths: 256 and 1024. Some settings have a sequence of 0, 4 or 8 inverters in order to evaluate the SEE electronic masking which occurs when a SEE is filtered by a combinational circuit. The shift registers have the following schematic:

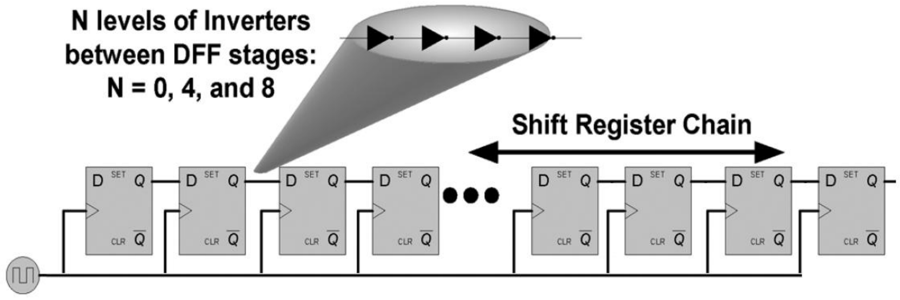

Fig. 3. Shift registers [4].

It permits analyze the SEE tolerance of the memory cells from the standard and rad-hard library.

- Transistors Set: The transistors set contains isolated transistors: both tolerant to radiation, such as non-tolerant. It allows the characterization of them in relation to TID and IxV curves. It is not tested as part of the technological payload.

In the NCBR1 context, only Pulse Generator and Shift Registers blocks are evaluated. The evaluation of the Transistors Set requires the use of micro-tips.

ASIC TEST AND INTEGRATION FOR CUBESAT

The SMDH Control block is an integral part of the synthesized FPGA circuit and implements the following features:

- Stimuli generation for the TC1;
- Capture and pre-processing of generated responses by TC1;
- Storage control responses on BRAM 1 block.

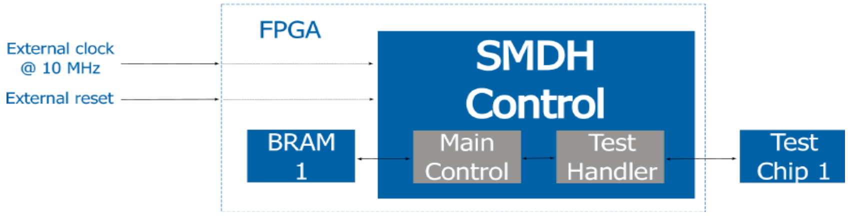

Fig. 4. SMDH Control block diagram.

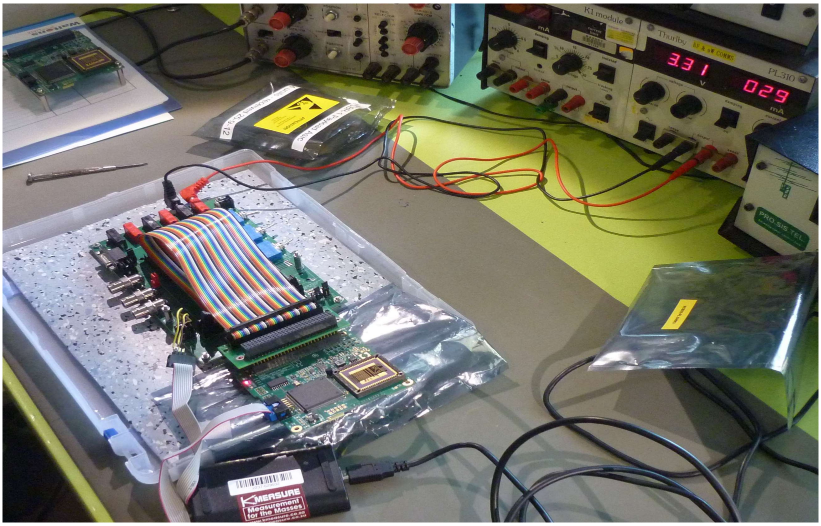

Fig. 5. Integration test.

The tests will be generated constantly from the time that the FPGA receive a configuration command after the reset. A timestamp is generated with a count that is only continuous during the tests. When the time arrives at the maximum count, a packet is sent with no error indication. This package is to ensure that the test environment is running and to keep the total execution time count of the tests.

Test	Bits response	Execution Time (us)
PG_ACTIVE	4	1920
PG_NO_PULSE	4	1920
PG_PULSE_OFF	4	1920
SR_PATTERN_GEN_ALT_256	5	1024
SR_PATTERN_GEN_ALT_1024	5	4096
Total	22	10880

Table 1. Tests generated by Test Handler.

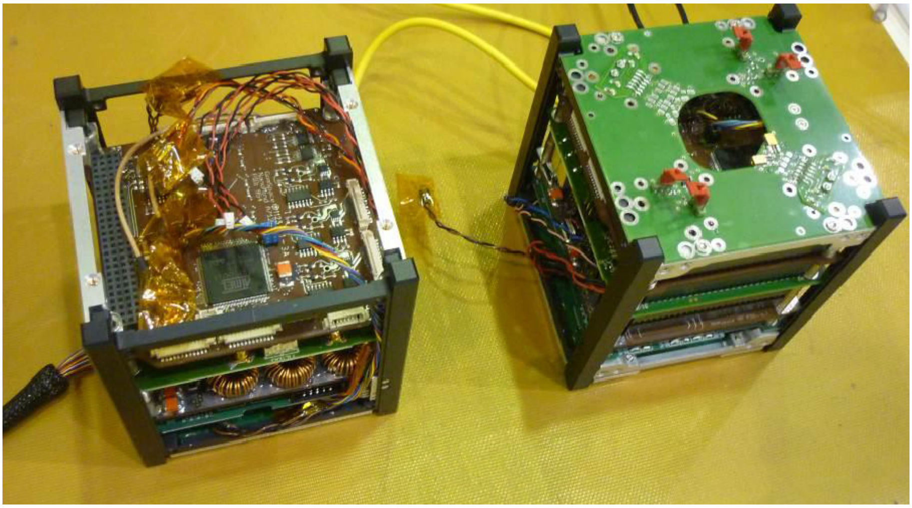

Fig. 7. Payload on NCBR1.

There are standards and specifications that must be followed for development and testing circuits to be tolerant to radiation effects. In the test was followed the set of rules and documents from ESA - European Space Agency, describing the test methods and evaluation of integrated circuits for space applications. The standard ESCC Basic Spec. No. 22900 - Total Dose Irradiation Steady-State Test Method [5] describes the procedures that should be followed to perform the ionizing radiation effects (TID) tests in ICs.

The circuit was designed to be tolerant to radiation effects and shall provide the same performance to the limit of requirements for which it was designed to operate. The shift registers was implemented to assess the effects of interaction with heavy ions that have enough energy to cause instantaneous events that can directly influence the circuit functionality.

Two types of SEE were evaluated in the tests:

- SEL - Single event latch-up: will be observed variation in the power supply. The occurrence of SEL is a condition characterized by causing loss of functionality of the device due to a single event (single event), caused by cosmic rays, for example, when induces a high current consumption. This type of event can cause permanent damage to the device, and requires that the circuit is turned off and then re-established the power to return to normal operation.
- SEU/SET - Single Event Upset/ Single Event Transient: the presence of errors in the output circuit will be observed. SEU/SET are characterized by the presence of errors observed in the operation of the circuit resulted by radiation caused by ions or electromagnetic energy in sensitive nodes of the integrated circuit structure.

RESULTS AND DISCUSSION

In all planned tests was possible to observe the errors caused by instantaneous radiation. In Table 2 is shown the characteristics of X-ray flux intensity with their respective severity level. This data is collected and monitored by the Geostationary Operational Environmental Satellite (GOES-15). Despite X-rays are not a main source of SEE in digital circuits, the increase in X-rays flux generally indicates the occurrence of a solar flare.

In Table 3 is shown the relation between SEE and the solar X-ray flux classified according with the Table 2. The highest severity levels R4 and R5 were omitted due no occurrences were reported during the experiment. At higher X-rays fluencies the number of SEE detected on the system increases. The measurement data shown that the IC was exposed to a high X-ray flux during the first two weeks of September 20014. These dates coincide with the strong solar flare that took place on 10 September 2014 which generated emissions of solar energetic protons (SEP).

Radio Blackouts			**GOES-X ray peak brightness by flux ***
R5	Extreme	Complete HF(High Frequency) blackout on the entire sunlit side of the Earth.	2 x 10-3
R4	Severe	HF radio communication blackout on most of the sunlit side of the Earth for one or two hours.	1 x 10-3
R3	Strong	Wide area blackout of HF radio communication, loss of radio contact for about an hour on sunlit side of Earth.	1 x 10-4
R2	Moderate	Limited blackout of HF radio communication on sunlit side, loss of radio contact for ten minutes.	5 x 10-5
R1	Minor	Weak or minor degradation of HF radio communication on sunlit side, occasional loss of radio contact.	1 x 10-5
* Flux, measured in the 0.1-0.8 nm range, in $W \cdot m^{-2}$. Based on this measure, but other physical measures are also considered.			

Table 2. NOAA Space Weather Scale for Radio Blackouts

Data Sets	Dates		#SEE detected	Data from EMBRACE # Events by severity		
	From	To		R1	R2	R3
1	20/06/14	30/06/14	0	0	0	0
2	01/07/14	12/08/14	996	6	1	0
3	12/08/14	13/08/14	297	0	0	0
4	13/08/14	15/08/14	17	0	0	0
5	15/08/14	17/08/14	88	0	0	0
6	17/08/14	19/08/14	146	0	0	0
7	19/08/14	23/08/14	170	0	0	0
8	23/08/14	23/08/14	1089	2	0	0
9	23/08/14	24/08/14	1338	1	0	0
10	25/08/14	27/08/14	1622	1	0	0
11	27/08/14	28/08/14	0	0	0	0
12	28/08/14	01/09/14	0	0	0	0
13	01/09/14	02/09/14	0	0	0	0
14	02/09/14	15/09/14	2529	6	1	1
15	15/09/14	16/09/14	0	0	0	0
16	09/22/14	09/22/14	0	0	0	0

Table 3. Total number of SEE detected in all shift-registers and pulse generator.

Figure 8 shown the SEE tolerance of two shift-registers with 256 stages and 8 inverters between each chain. The blue bar corresponds to the shift-registers designed using the conventional digital cells provided by the foundry. On the other hand, the red bars represents the radiation hardened digital cells designed by SMDH. It is remarkable to mention that radiation hardened cells designed by SMDH proved tolerance to SEE with X-rays events of severity R1 and R2. In relation to the R3 event, the designed cells reported some errors by SEE. The amount of errors in the shift-registers designed using the standard cell library is comparatively larger than the shift-registers using rad-hard cell library.

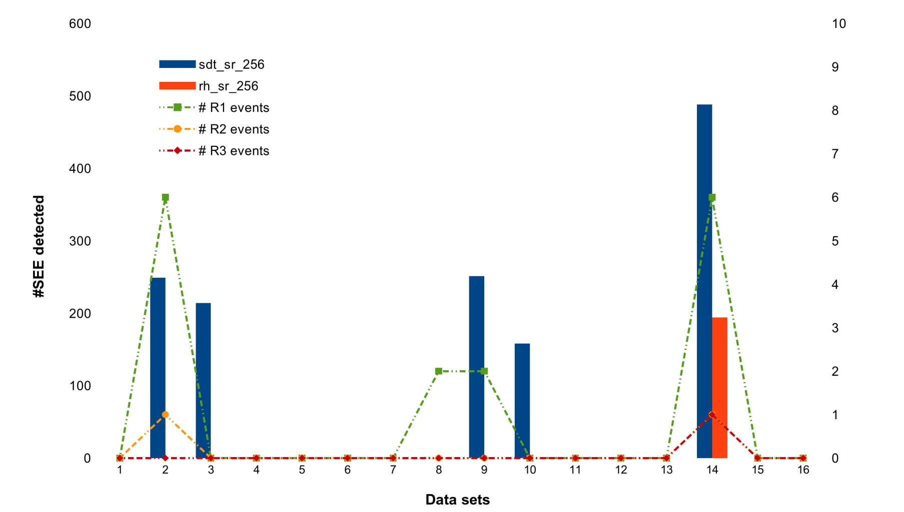

Fig. 8. SEE tolerance comparison of two shift-registers (256 FF, 8 INV).

In order to analyze and quantify the energy levels measured during the R3 occurrence and thus estimate the tolerance of customized cells, in Figure 5 is shown the fluency of SEPs during September 2014 at different levels of energy. During the first two weeks were reported SEPs with energies above 100MeV.

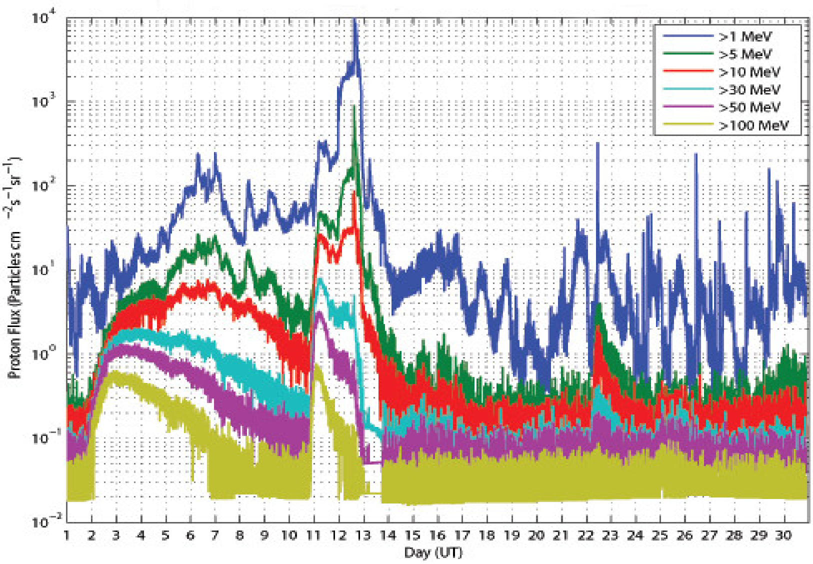

Fig. 9. Solar energetic protons detected by GOES-15 satellite during September 2014.

CONCLUSION

The NanoSatCBR1 project developed by INPE and UFSM partnership demonstrated an excellent alternative to consolidate Brazilian space industry. The radiation hardened digital cells designed by SMDH proved a tolerance to solar energetic particles of energies of up to 100MeV. Additionally, the data analysis from GOES-15 satellite allows to relate the X-rays flux with the occurrence of SEE in the integrated circuits. Despite the X-rays originated in solar flares are not the cause of reported SEEs, they are linked with the emission of solar energetic particles (SEP) after a solar flare. This particles travel from the Sun to the Low Earth Orbit and impacts the satellite circuitry. The experiment results exposed the systems effects of the outer space and demonstrated the challenge of design integrated circuits to this radiation environment.

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