Specifications for a Multi-Standard SBCD/ARGOS-3 Integrated UHF Satellite Receiver

C. C. A. Mendes[1 3], G. C. L. Cunha[1 3], M. Vasilevski[1 3], V. Bourguet[1], S. Y. Catunda[1], R. N. Lima[2], M. Barros[3]
[1]Department of Electrical Engineering, UFRN, Natal, RN, Brazil
[2]Department of Electrical Engineering, UFBA, Salvador, BA, Brazil
[3]National Institute for Space Research, INPE-CRN, Natal, RN, Brazil

***Abstract*—The specifications for the front-end design of a SBCD/ARGOS-3 integrated UHF receiver in a 0.13 μm stardard CMOS process are derived. A low intermediate frequency architecture is presented, in which a 3-stage low-noise amplifier, a passive mixer and a phase-locked loop based frequency synthesizer are employed for achieving the resulting specs.**

***Index Terms*—ARGOS-3, SBCD, UHF Receiver, CMOS**

I. Introduction

The Brazilian System of Data Collection (SBCD) [1] and ARGOS-3 [2] are satellite-based environmental data collection systems. They perform *in situ* measurements [3] by receiving data retransmitted from autonomous Data Collection Platforms (DCPs) through satellites. Both systems consist of three segments, one in space and two on ground. A satellite constellation composes the space segment, whereas reception ground stations and the DCPs constitute the ground ones. The DCPs use sensors to capture environmental data, that is packetized and transmitted in an UHF uplink to the Low Earth Orbit (LEO) satellites. Afterwards, the ground stations are in charge of demodulating the signal and recovering the data received from the satellites in a S-band downlink. The final user utilizes the retrieved *quasi* real-time data for general environmental analysis, e.g., oceanography, meteorology, monitoring wildlife, volcanoes, fishing fleets, managing water resources, and so on [4].

The ARGOS system is world widely used for providing data acquired from oceanography buoy and mobile platforms, such as marine mammals and vessels. The program ARGOS started off in 1974 out of a cooperation among the French National Centre for Space Studies (CNES), the U.S.A. National Aeronautics and Space Administration (NASA) and the U.S.A. National Oceanic and Atmospheric Administration (NOAA) [2]. Currently, it consists of 60 ground stations and more than 21000 platforms spread all over the world.

SBCD is the keystone for monitoring the huge Brazilian territory through the collection of environmental data in a multitude of domains like meteorology, hydrology, animal monitoring and fire prevention [5]. The SBCD was based on the ARGOS system and it was deployed in 1993 with the launching of the satellite SCD-1. Nowadays, the system is composed by more than 800 PCDs being used by over 100 organizations [6].

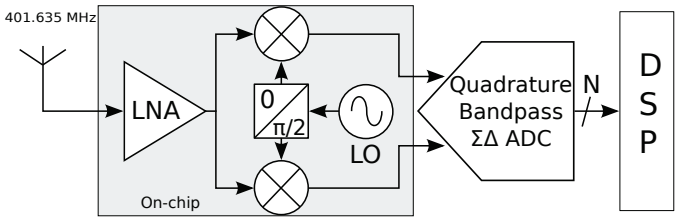

Fig. 1: Multi-Standard SBCD/ARGOS-3 UHF receiver.

This paper aims at presenting the detailed specifications for the design of an integrated CMOS multi-standard receiver which supports both systems, SBCD and ARGOS-3. It is relevant to mention there are no papers about SBCD and ARGOS co-work design so far. Thus, this work intends to establish a reference for such collaboration. Due to the intrinsic challenges encountered in satellite electronic systems design, such as cost and energy consumption, a low-IF receiver is proposed for such design (Fig. 1). This architecture includes a quadrature bandpass Sigma-Delta ADC [7], [8] that digitizes the band of all the transmission modes of both SBCD and ARGOS-3 systems.

The structure of the paper is organized as follows. In Section II, we present the requirements of SBCD and ARGOS-3 systems. Then, Section III describes the UHF receiver specifications that have been computed by considering the most critical reception scenario. Finally, in Section IV we detail the proposed topologies of the Low-Noise Amplifier (LNA), the mixer and the Local Oscillator (LO) for the UHF receiver front-end.

II. System Requirements

The ARGOS-3 system defines two transmission modes depending on the targeted applications. These are Low Data rate (LD) and High Data rate (HD). Moreover, LD mode is subdivided into Standard Service (STD) and High Sensitivity Service (NG). SBCD and each mode of ARGOS-3 specify the physical layer requirements, namely data rate, data coding, RF modulation, bandwidth occupation and signal power constraints which are presented in Table I. For instance, in

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TABLE I: ARGOS-3 and SBCD requirements for the uplink receiver.

Parameters	SBCD	ARGOS-3		
		High Data rate (HD)	Low Data rate (LD)	
			(STD)	(NG)
Sensitivity	-123 dBm	-123 dBm	-123 dBm	-137 dBm
$P_{in,max}$	-98 dBm	-108 dBm	-114 dBm	-114 dBm
$f_{central}$	401.635 MHz	401.595 MHz	401.650 MHz	401.650 MHz
Bandwidth	120 kHz	30 kHz	80 kHz	80 kHz
Bit Rate	400 bps	4800 bps	400 bps	400 bps
Coding	Biphase-L	Conv.(7,3/4)	Biphase-L	Conv.(7,1/2)
Chips Rate	800 cps	6400 cps	800 cps	800 cps
Modulation	PCM/PM/ $\pm 60^\circ$	GMSK	BPSK	QPSK

the ARGOS-3 HD mode the physical data is sensed by the DCPs producing a bit stream operating at 4800 bps, it is then encoded using a $(7,\frac{3}{4})$ convolutional code and transmitted employing Gaussian Minimum Shift-Keying (GMSK) modulation at 401.595 MHz. Then, the uplink receiver embedded into the satellite must ensure the signal is properly detected within the 30 kHz band centered at 401.595 MHz. In order to achieve a Bit Error Rate (BER) less than 10^{-5} the received signal power must be within the constraint range of [-123 dBm; -108 dBm].

III. Front-End Specifications

Since a multi-standard receiver is proposed, several reception scenarios have to be foreseen. Depending on the specification which is evaluated, a given scenario applies. Concerning the front-end Noise Figure (NF), gain and iCP1 the reception of an ARGOS-3 HD signal is considered for it employs a more sophisticated modulation scheme and thus requires a more detailed analysis. On the other hand, since the ARGOS-3 LD NG signals are the weakest, they are regarded for deriving the LO phase noise and spurious requirements. Moreover, the receiver must cover a 120 kHz bandwidth centered at 401.635 MHz so as to accommodate all SBCD and ARGOS-3 bands.

A. Noise Figure

The SNR at the receiver input can be computed as the ratio between the receiver sensitivity and the noise power in the signal bandwidth [9]. Moreover we consider an additional insertion loss (IL) of 1.5 dB for the external components preceding the LNA, namely, a switch, a bandpass filter and a balun.

$$SNR_{in} = Sensitivity - IL - 10\log_{10}\left(\frac{kTB}{0.001}\right) \quad (1)$$

In order to design a robust receiver we must regard the worst case of the temperature (T), which varies from -10 to 50°C. Concerning the signal bandwidth, it is important to quantify the impact the coding rate (ρ) and the modulation scheme spectral efficiency (τ) have on it [10], respectively increasing and decreasing its value as expressed in Eq. (2) and (3):

$$\tau = \log_2(M)/(1+\alpha) \quad (2)$$

$$B = \frac{R_b}{\tau \times \rho} \quad (3)$$

where M is the constellation density, α is the roll-off factor of the Gaussian Filter in GMSK modulation and R_b is the data rate. Thus evaluating Eq. (2) and (3) into Eq. (1) we compute the SNR_{in} as in Eq. (4).

$$\begin{aligned} SNR_{in} &= -123 - 1.5 - 173.5 + 10\log_{10}\left(\frac{4800}{3/4 \times 4/3}\right) \\ &= 12.2 \text{ dB} \end{aligned} \quad (4)$$

From the signal modulation and the required BER, we calculate the minimum SNR the receiver must achieve:

$$SNR_{out} = E_b/N_0 + 10log(R_b/B) \quad (5)$$

where the E_b/N_0 is the energy per bit to noise power spectral density ratio, obtained from a system-level simulation. Finally, we consider a 0.5 dB margin and compute the NF that gives the noise budget for the receiver design:

$$\begin{aligned} NF &= SNR_{in} - (SNR_{out} + Margin)(\text{dB}) \\ &= 12.2 - [5.2 - (0) + 0.5] = 6.5 \text{ dB} \end{aligned} \quad (6)$$

B. Gain

The front-end gain is computed in order to fit the input signal within the ADC dynamic range, respecting the SNR_{out} the receiver must achieve for the desired BER. From the ADC specifications shown in Table II, it is possible to compute the ADC Noise Floor as:

$$ADC_{noise} = -5.2 - (16 \times 6.02 + 1.76) = -103.25 \text{ dBm} \quad (7)$$

A design choice is to neglect the ADC noise regarding the noise power added by the previous blocks. Hence, we consider a margin of 10 dB between the ADC quantization noise and the referred receiver noise, which leads to the required gain G for the receiver front-end as follows:

$$\begin{aligned} G &= ADC_{noise} + ADC_{margin} + SNR_{out} - Sensitivity \\ &= -103.25 + 10 + 5.7 - (-124.5) = 37 \text{ dB} \end{aligned} \quad (8)$$

C. Linearity

The worst case approach indicates one must consider the highest value between two ways of computing the iCP1. The first one takes into account the highest power blocker (-72.5 dBm @ 462.5 MHz) [5] present in both systems dropped by 1 dB plus a 3 dB margin (Eq. (9)); and the second one backs-off the ADC reference level by the required gain (Eq. (10)).

$$iCP1_{blck} = P_{blck,max} + 3 - 1 = -70.5 \text{ dBm} \quad (9)$$

$$iCP1_{adc} = ADC_{ref} - G = -42 \text{ dBm} \quad (10)$$

TABLE II: Partial ADC specifications for a bandwidth of 40 MHz centered at 22 MHz.

Resolution (N)	16 bits
Reference Level	-5.2 dBm
Noise Margin (ADC_{margin})	10 dB

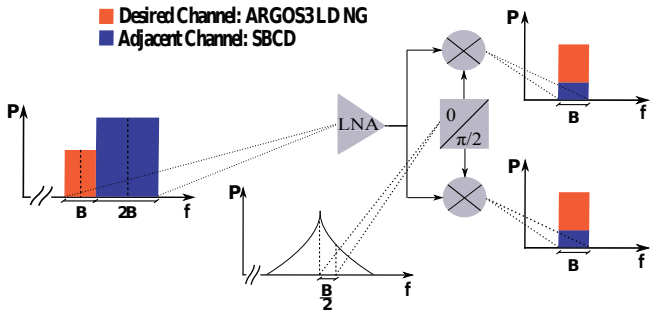

Fig. 2: Worst case scenario for an ARGOS-3 LD NG channel reception.

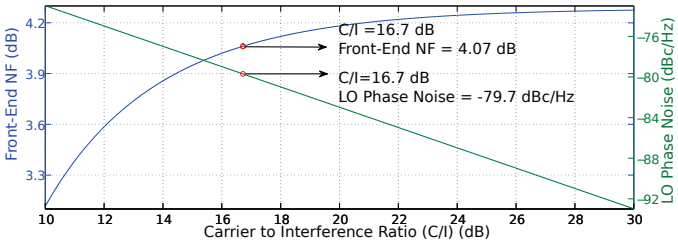

Fig. 3: Evaluation of LO phase noise, front-end NF and C/I.

D. LO Phase Noise and Spurious

The reciprocal mixing of an adjacent channel with the LO phase noise will dictate the carrier-to-interference (C/I) ratio, which in turn, degrades the BER [11]. In fact, it is possible to establish a relationship between C/I, the LO phase noise at a certain frequency offset ($L(\Delta f)$) and the front-end NF required for a given reception scenario, as defined by Eq. (11) and (12), [12], [13]. P_{des} and $P_{adj}(\Delta f)$ are the power of the desired and adjacent channels, respectively.

$$L(\Delta f) = P_{des} - P_{adj}(\Delta f) - \frac{C}{I} - 10\log_{10}(B) \qquad (11)$$

$$F = \frac{SNR_{in}}{SNR_{out}} - \frac{P_{adj}(\Delta f)L(\Delta f)}{kT} \qquad (12)$$

For the reception of an ARGOS-3 LD NG channel for instance, the most critical scenario concerning the LO phase noise requirement is illustrated in Fig. 2. In such scenario, B = 0.5 kHz and P_{des} = -137 dBm. Even though the maximum power of a SBCD channel is -98 dBm, its bandwidth is double the ARGOS-3 LD NG one. Therefore, $P_{adj}(\Delta f)$ = -101 dBm. Furthermore, SNR_{out} = 3.7 dB guarantees a BER of 10^{-5} for the ARGOS-3 LD NG channel reception. According to Eq. (1), SNR_{in} = 8 dB for T = 50 °C and finally G = 49 dB as presented in Table III.

For the case of Fig. 2, the relationship between C/I, LO phase noise and NF front-end is presented in Fig. 3. A stringent requirement of C/I, say 30 dB, requires a LO phase noise lower than -90 dBc/Hz at an offset of 0.25 kHz [11], which is rather stringent. However, it is possible to trade-off the front-end NF for a more relaxed LO phase noise requirement. In fact, backing-off the front-end NF in about 5%, from 4.3 to 4.07 dB, reduces C/I to 16.7 dB which relaxes the required LO phase noise to -79.7 dBc/Hz. A complete analysis of the LO phase noise requirements as well as the $NF_{LO_{noise}}$, which is the NF required considering the LO phase noise, is obtained by repeating the aforedescribed procedure for the worst case reception of the SBCD and the remaining ARGOS-3 channels.

TABLE III: Receiver specifications.

Parameters	SBCD	ARGOS-3		
		High Data rate (HD)	Low Data rate (LD) (STD)	Low Data rate (LD) (NG)
G	38.3 dB	37 dB	34 dB	**49 dB**
NF	12 dB	6.5 dB	18.3 dB	**4.3 dB**
$NF_{LO_{noise}}$	11.36 dB	6.15 dB	17.32 dB	**4.07 dB**
iCP1	-43 dBm	**-42 dBm**	-43 dBm	-43 dBm
L(Δf)	-70.8 dBc/Hz @ 0.5 kHz	-78.7 dBc/Hz @ 2.4 kHz	-70.8 dBc/Hz @ 0.5 kHz	**-79.7 dBc/Hz @ 0.25 kHz**
P_{spu}	-57.5 dBc	-56.2 dBc	-54.2 dBc	**-68.2 dBc**

The LO spurious requirements are derived on the basis of the highest power blocker. Eq. (13) shows the result for the reception of the ARGOS-3 LD NG channels.

$$\begin{aligned} P_{spu} &= P_{des} - P_{blck,max} - SNR_{out} \\ &= -137 - (-72.5) - 3.7 = -68.2\text{dBc} \end{aligned} \qquad (13)$$

Finally, the previous calculations are extended to all scenarios and the results are gathered into Table III. The highlighted values represent the worst cases and should be considered while designing a multi-standard SBCD/ARGOS-3 low-IF receiver.

IV. Front-End Design

A. LNA

The gain of 49 dB is realized using a LNA with three stages [14]. The first stage (Fig. 4 (a)) is the most critical, because it must realize the impedance matching to maximize the power delivered to the chip (S11 < -10 dB), and amplify the signal with a small NF to relax the constraints on the noise for the subsequent stages. A Power-Constrained Simultaneous Noise and Input Matching (PCSNIM) technique is used in order to achieve a good compromise between high gain, input impedance matching, low NF and low power consumption at the same time [15]. The addition of the C_{ex} capacitor to the traditional Simultaneous Noise and Input Matching (SNIM) technique, allows the circuit to work at low power consumption without influencing the Minimum NF nor the Noise Resistance [16]. A low-noise LC tank loads the stage and slightly attenuates the blockers. Due to size issues, the second and the third stages (Fig. 4 (b)) consist of inductorless cascode topologies with a resistive load. Their induced noise is higher, but its effect is reduced by the gain of the first stage. In Table IV we summarize the LNA specifications.

B. Mixer

In order to easily achieve the requirements on linearity (Table III), we use a passive mixer (Fig. 5), which is ideally noiseless and linear. Due to stringent requirements on linearity (Table III), we use a passive mixer (Fig. 5), which is ideally noiseless and linear. The conversion losses of this topology

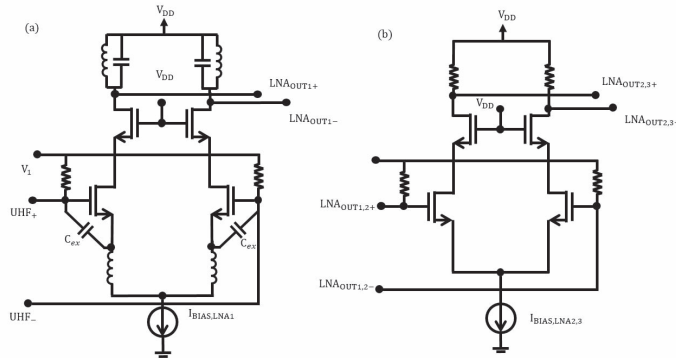

Fig. 4: The multiple-stages LNA: the first stage (a), the second and third stages (b).

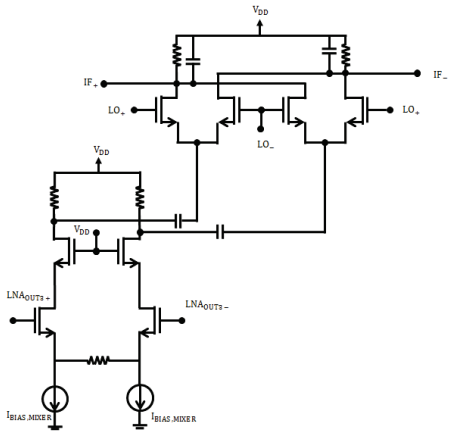

Fig. 5: The passive mixer with its input buffer.

are compensated by using a buffer at the mixer input [17]. The buffer adds noise and non-linearity, but with a cascode structure it helps to isolate the LNA from the varying mixer input impedance. The conversion gain is determined by the buffer transconductance, the coupling capacitor, the switches R_{on} and the first filter stage that loads the mixer. The requirements to guarantee the specified image-rejection ratio must be validated through the good matching of the inphase and quadrature mixers. In Table V we summarize the Mixer specifications.

C. Local Oscillator

In order to guarantee frequency stability in a harsh environment, a PLL-based frequency synthesizer might be considered. The receiver bandwidth is centered at 401.635 MHz and the LO frequency should be within the following range 403.635 MHz $< f_{LO} <$ 420.5 MHz. It ensures the highest power blocker is kept outside the ADC bandwidth, which is a 40 MHz band centered at 22 MHz, after down-conversion. The receiver requires a single LO frequency, thus for the sake of simplicity a N-integer PLL is the most suitable choice.

V. Conclusion

This work is meant to be a reference on the design of integrated UHF receivers for two of the most important *in situ* data collection systems in the world, SBCD and ARGOS-3. The detailed specifications of a multi-standard receiver were derived and a low-IF architecture proposed. Besides, LNA, mixer and PLL topologies were discussed considering the important trade-offs involved in the design of this UHF integrated receiver. Finally, the next steps of the project aim at continuing the design and later on manufacturing and characterizing the proposed receiver in a 0.13μ standard CMOS technology.

TABLE IV: LNA specs.

Input Frequency	401.635 MHz
NF	$<$ 4.3 dB
Gain	$\geq$ 49 dB
S_{11}	$<$ -10 dB
iCP1	$\geq$ -42 dBm

TABLE V: Mixer specs.

LO Frequency	403.635-420.5 MHz
IIP3	$\geq$-34 dBm
Conversion Gain	0 dB
I/Q phase dif.	3°
I/Q gain dif.	3%

Acknowledgments

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