Timestamp Reliability of the Schenberg Gravitational Wave Detector Data Acquisition System

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***Abstract*— The Schenberg gravitational wave (GW) detector has been under development for the past few years. A scientific run is planned for the near future. The main technique used to confirm a GW is the search for time coincident events between multiple detectors. Therefore, a reliable timestamp is essential for events found in data from each detector. In the particular case of the Schenberg detector, we are planning a low latency analysis, which requires that no data sample be lost during either data acquisition (DAQ) or transmission, and that time correction be done online. The aim is to provide reliable data where each sample carries its own timestamp information. GW event candidates are pointed out after a dedicated analysis and their time of occurrence are determined by these samples. We present here the DAQ solution developed for the Schenberg detector. It is easy to implement this solution using equipment commonly found in most laboratories. No specific equipment using precision time protocol or other protocol was needed to synchronize the sampling. In addition, no transmission time is needed to be explicitly known. The timing precision is limited only by the chosen sampling frequency, which fulfills the data analysis needs.**

***Index Terms*— Astronomy, data acquisition (DAQ), detectors, synchronous detection, timing.**

I. Introduction

SCHENBERG is a gravitational wave (GW) detector, which uses a spherical resonant mass with a high mechanical quality factor $Q \sim 10^7$. The sphere's mass and diameter are 1150 kg and 65 cm, respectively, which leads to a resonant frequency $f_0 \sim 3.2$ kHz. GWs couple to the sphere's five quadrupolar modes [1], [2]. The sphere's mechanical oscillations are then converted into electromagnetic signals by six resonant transducers with klystron-type cavities [3]. A 10-GHz microwave signal is pumped into the resonant cavity and modulated by its oscillations ($df/dx \sim 0.5$ GHz/μm) [4], [5]. This signal is then demodulated, amplified, and digitized for subsequent analysis.

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A high precision timestamp and strict data continuity are two critical requirements for GW data analysis. The most common procedure to confirm GW detection is a coincidence blind search between multiple detectors. If coincident signals, above SNR ∼5, happen to be found in three detectors, in a typical time window of 1 s, the probability of a false positive would be $1/10^4$ year.[1] The time window depends on each detector's time resolution. Thus, the better the time resolution, the lower the false alarm rate is [6]–[9]. The previous resonant mass detectors NAUTILUS, EXPLORER, and Allegro provided a precision of 12.8, 6.4, and 8 ms, respectively [6], [10].

Previously, data timestamp corrections were performed during offline analysis. In the present case, we are aiming at a low latency analysis with a delay <1 s for 30 s of data [11]. Therefore, all corrections need to be executed online.

Another point is the search for periodic signals. In this kind of research, any sample lost or time shifted might be interpreted as a frequency shift or power loss of the source signal [12]–[14].

Protocols as network time protocol (NTP) [15], [16], precision time protocol (PTP) [17]–[19], and white rabbit (developed at CERN) [20], [21] allow the synchronization of clocks within a defined network in the respective ranges of ∼10 ms, sub-μs, and ns. In our case, a GPS receiver is already integrated in the data acquisition (DAQ) system and there is no need to propagate the synchronization to other systems.

These protocols are perfect to timestamp discrete events (considering electronic delays). For example, we keep a record of cosmic ray showers hitting the detector and use NTP to mark their timestamps [22].[2] In the case of potential GW signals, we need to perform many transformations (Fourier transform and its inverse, aliasing, filters, and others) on the data before timestamping a potential GW event. Therefore, it is easier for the GW analysis if each sample carries the timestamp information in the same way, for example, such as the one used in very long base interferometry [23], where the sampling is synchronized with integrated systems of high-frequency clocks and GPS. The GW detector

[1] The threshold SNR vary in function of the noise of each detector.

[2] The cosmic ray veto is presently connected to another DAQ system. The two DAQ evolve separately, their data are completely different.

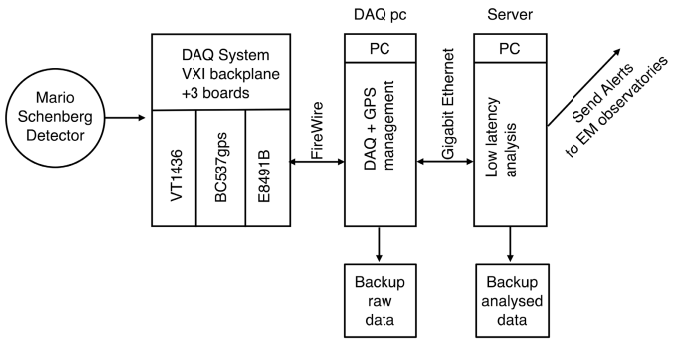

Fig. 1. Schematic of the DAQ setup. Analog-to-digital conversion is done by a VTI Instruments VT1436 board. Time reference is provided by a TFP BC537gps from symmetricom. Finally, the bridge between VXI backplane and DAQ PCs is performed by an Agilent board E8491B.

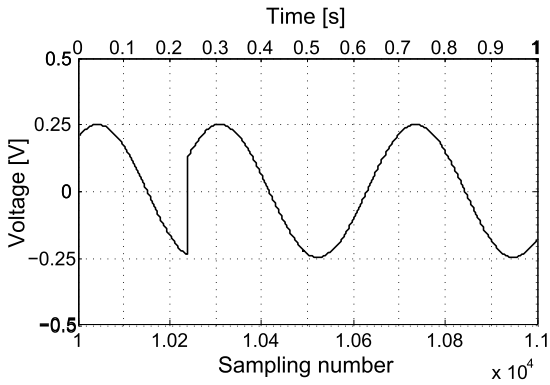

Fig. 2. Data loss due to the block mode. We used a signal generator with a sinusoid of 60 Hz to check the continuity of our DAQ. Sampling is 25 kHz.

LIGO has developed its own boards with high-frequency clocks (∼8.4 MHz) to provide synchronized sampling [24]. In our case, we can indeed use one of the above methods to timestamp our samples, principally the PTP. One approach is to use analog-to-digital converters (ADCs) based on the LXI standard (class B or C), which are compatible with PTP. However, we need to maintain a legacy VXI system, which is not compatible with this protocol. In addition, currently, there are only a few vendors providing analog-to-digital boards with timestamped data, as shown in the LXI product page [25].

Therefore, GW data analysis does not need a better time resolution than the one given by the sampling rate. Then, preserving the existent equipment, we present here a solution where the sampling is synchronized with a conventional time frequency processor (TFP) clock, which is itself synchronized with GPS pulse per second (PPS). The Schenberg detector DAQ setup (ADC, TFP/GPS, and VXI-PC board) is described in Section II. It is configured to provide a data stream without any interruption.

In previous measurements, we encountered technical problems that appeared as data loss. This problem, along with its solution, is described in Section III. Once we ensured data continuity, we synchronized the sampling with GPS PPS (Section IV). To conclude this method, a technique to retrieve the timestamp using PPS signal recorded by the ADC is described in Section V.

II. DAQ Setup

The Schenberg DAQ system is based on a VXI CT-400 backplane, as shown in Fig. 1. The CT-400 chassis has 13 slots, where three of them contain the boards (C-size industry standard).

Time reference is provided by an Symmetricom TFP BC537gps. It uses an external GPS to provide the time with a precision of 1 μs. In case of GPS signal loss, its internal clock assumes the relay. During DAQ, we record an extra channel containing its PPS signal. As shown below, the TFP also drives the ADC external trigger.

Transducer signals are digitized by an ADC VT1436 board from VTI Instruments. It provides 16 channels with a maximum sampling of 102.4 kSa/s and a DRAM memory buffer of 32 MB (16 MSa) divided by the number of channels. Each sample is 2-B long. Seven channels are used for the transducer signals and one for the PPS signal. The remaining channels will be used for auxiliary sensors (i.e., seismometers, magnetometers, and voltmeters).

The interface between VXI backplane and DAQ PCs is performed by an Agilent board E8491B. The data are transferred via industry standard IEEE-1394 bus (firewire, 400 Mb/s).

One PC is fully dedicated to DAQ, whereas another PC is used as a server and to perform the real-time analysis. The low latency pipeline accesses the data stream generated by the DAQ software. The data are transferred for analysis with their own timestamps.

A. DAQ Software

Using MATLAB, a software, named SDAQ, with a graphical user interface to manage the DAQ was written.[3] It allows the user to set parameters, such as channel selection, sampling rate, voltage range and data block size, and displays the acquisition status. It also provides two online data displays: 1) spectrum analyzer and 2) oscilloscope.

When starting the DAQ, the program automatically configures the TFP and the ADC with predefined parameters.

III. Continuity of the Data

The ADC works on a first in, first out principle. The transmission from the ADC buffer to the PC is performed by sending data blocks of different possible sizes, such as 1024, 2048, and 4096 samples. It is possible to transfer these blocks using two different modes.

In the block acquisition mode, the system waits until the data are transferred before continuing the acquisition. If the command that asks for the data transfer is delayed, data blocks are not collected during this period, and are, therefore, lost, as shown in Fig. 2. There are different reasons why this delay can happen, but it is mainly due to the time lag when sending the request of a new block synchronously with the acquisition.

In the continuous acquisition mode, the data are continuously acquired independently of the transfer command.

[3]LabView could be seen as a better environment to develop a DAQ program, but our choice was due to logistic and practical reasons.

TABLE I
MAIN PARAMETERS OF THE TWO TESTED SIGNALS

Signal	Sine (100 Hz)	Ramp (5 s)
Sampling [kHz]	25	25
Block size [samples]	1024	1024
Number of blocks per file	500	500
Number of files	2110	2110
Number of PPS	43213	43213
Total time [s]	43212,8	43212,8

This mode avoids the previous problem, but it has two issues depending on the number of data blocks to be transferred. If the chosen number of data blocks is too small, the blocks will be ready before the software sends the request to acquire them. After a while, the buffer capacity will be exceeded and data are lost. If the number of blocks is excessive, we can also overload the buffer.

The data transfer from the ADC board to the DAQ PC takes 17.3 ± 4.5 ms. Therefore, the DAQ time should be longer than this. Therefore, we round the transfer time to 22×10^{-3} s and the minimum number of samples is given by

$$\mathrm{NS}_{\min} = 22 \times 10^{-3} \cdot f_s \tag{1}$$

where NS is the number of samples and f_s is the sampling frequency [Hz]. Then, the minimum number of blocks NB is given by

$$\mathrm{NB}_{\min} = \frac{22 \times 10^{-3} \cdot f_s}{\mathrm{bs}} \tag{2}$$

where bs is the block size. The maximum number of blocks is

$$\mathrm{NB}_{\max} = \frac{16 \times 10^{6}}{8\mathrm{bs}} \tag{3}$$

where we considered eight channels and 16×10^6 is the buffer size in sample number. The DAQ sampling rate is $f_s = 15\,625$ Hz, which implies, using a block size of 1024 samples, that the minimum number of blocks is 1 and the maximum number is 1953.

A. Testing the Continuity

We tested the DAQ continuity by measuring two different signals. First, we applied a low-frequency ramp signal with a period of 5 s. Then, we measured a sinusoidal signal with a frequency of 100 Hz. Both signal amplitudes were 5 V peak-to-peak. In both the cases, the PPS signal was recorded at the same time. In Table I, we report the main parameters of these two tests with the number of PPS measured.

1) Test Using a Ramp Signal: This test serves to check the software management of acquisition. If there is a discontinuity, it should happen between block transfer and, therefore, be shown as steps on the ramp. No such feature was observed.

2) Test Using a Sinusoidal Signal: We recorded 2110 files containing 500 data blocks of 1024 samples, equivalent of ~12 h, with a continuous 100-Hz sinusoidal signal. We used a higher sampling frequency (25 kHz) instead of 15 625 Hz to stress the system. With a higher sampling frequency, the data loss conditions (overload) mentioned above is reached faster.

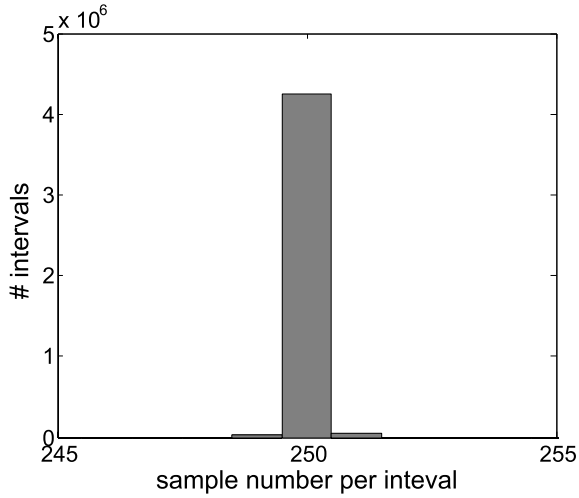

Fig. 3. Number of bins per period. Sampling is 25 kHz and the signal frequency is 100 Hz.

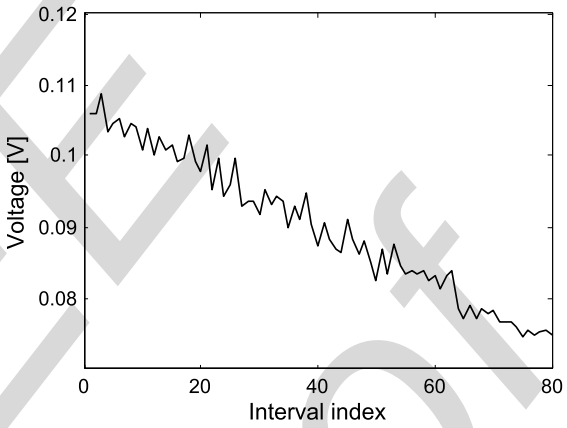

Fig. 4. Value of the first samples of 80 periods.

In Fig. 3, we report the measured number of samples per period, which should be sampling/signal frequency = 25 000/100 = 250. The total expected sample number is 1 080 320 000. We measured $4\,249\,024 \times 250$ samples, $29\,100 \times 249$ samples and 43100×251 samples, which gives a total of 1 080 320 000 samples. No data were lost.

In order to understand the number of sample deviation, we performed a fast Fourier transform of the signal over 211 files and got a frequency of 99.9986 Hz and, therefore, the period is 250.0035 samples. This value is confirmed by dividing the number of data by the number of periods that we obtain, the period lasts 250.003 samples. We also tested the first nonzero value of 80 consecutive sine periods (Fig. 4). There is a slight decrease in these values at every 250th sample, which means that each time the signal period is starting earlier than the previous period and thus the signal period is >250 samples. Actually, we will see below that the sampling rate is also not regular. This irregularity can also contribute to this variation.

IV. SAMPLING REGULARITY

In order to use the number of samples and PPS to provide timestamps, the sampling rate should be constant between pulses.

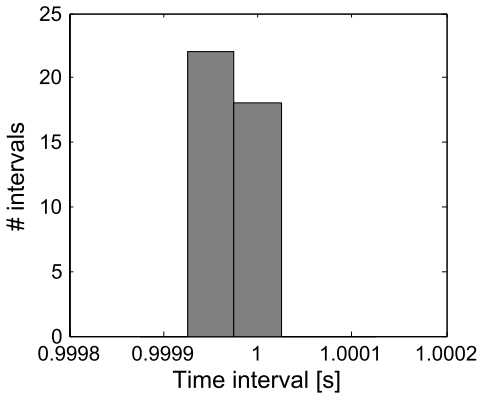

Fig. 5. Histogram of 40 pulse intervals obtained from a 40 s acquisition. Each bin represents 39 μs.

The ADC VT1436 can either use its internal clock or an external one to generate sampling frequencies. The range of available internal clock frequencies is from 40.96 to 102.4 kHz. In both the cases (internal or external clocks), sampling frequencies are defined as the set clock frequency divided by 2.56. From these primary sampling frequencies, the ADC generates other ones by dividing them either by 5 or by powers of 2 or by both.

We noticed that when the internal clock was used, the ADC sampling rate was not constant between two consecutive pulses. For example, we set the sampling rate to 25 kHz and counted the number of samples between pulses.[4] The result of 40 s of acquisition is shown in Fig. 5. Around half of the pulse intervals had smaller sample counts than the expected 25 000. After 24 h, the accumulated delay was ~1.7 s. This is an excessive shift for the analysis, remembering that the coincidence search is typically performed within a 1 s window. Therefore, the number of samples could not be used as a marker to count time intervals.

A. Using TFP Clock to Drive ADC Clock

Since the GPS receiver has a 1-μs precision, which is smaller than the sampling rate, we use the TFP internal clock to drive the ADC sampling.

1) Connecting the TFP BC537gps and the ADC VT1436: The average measured voltage of the TFP BC537gps clock are ~3.9 and ~0.1 V, at the highest and lowest levels, respectively, which are transistor–transistor logic compatible as required by the ADC VT1436. Therefore, neither amplification nor attenuation was needed. All tests described below were performed using this signal.

We used the external sample SubMiniature version B connector (SMB) connector on the ADC front panel to connect the external clock. The TFP output is a 15 pin D socket. Therefore, we built a 15 pin D plug to SMB adapter, which connects both boards (Fig. 6). This adapter actually carries both signals: 1) the PPS and 2) the external clock.

The TFP driving clock can be programmed to fit the ADC range by the following expression: 1) $f_{\text{clk}} = 10\ \text{MHz}/(n_1 \times n_2)$, where 10 MHz is the TFP BC537gps internal clock and 2) n_1 and n_2 are two programmable values. For example, to achieve 100 kHz, $n_1 = 2$ and $n_2 = 50$. The clock frequency generated by the TFP is chosen to match an internal ADC one to avoid radical changes in the sampling rate in the case of a system failure. If the ADC loses the external clock, it will use the closest internal sampling frequency available. The frequencies generated by the TFP that match the ADC VT1436 internal frequencies, and which are between the admissible range (40.96–102.4 kHz), are: 50, 62.5, 78.125, 80, and 100 kHz.

[4]The number of samples was also tested with many others sampling frequencies. In all cases we found a deviation in the number of samples between pulses.

Fig. 6. Picture showing the three boards. BC537gps is located in the middle where one can see the 15 pin D plug with two cables (PPS and the external clock signals) leaving it. Just above it, the cable to the GPS antenna can be seen. VT1436 board is on the right and the E8491B board is on the left.

The Schenberg resonant frequency is ~3.2 kHz and, therefore, the sampling rates need to be >6.4 kHz. Considering the external and internal clock compatibility and the sampling constrains, we have implemented the following list of sampling frequencies, such as 10, 12.5, 15.625, and 20 kHz. For our measurements, we are using 15.625 kHz. This choice is justified by a compromise between an improved time resolution, 64 μs, with respect to previous experiments (~10 ms) and to avoid an excess production of unnecessary data, which will slow down the analysis.

2) TFP Periodic Signal and PPS Signal Synchronization: The clock signal generated by the TFP can be synchronous or asynchronous with the PPS, as shown in Fig. 7. In order to control the number of samples between pulses, we use the synchronous mode.

B. Testing the Sampling Regularity

After having connected the two boards, we executed the following two tests.

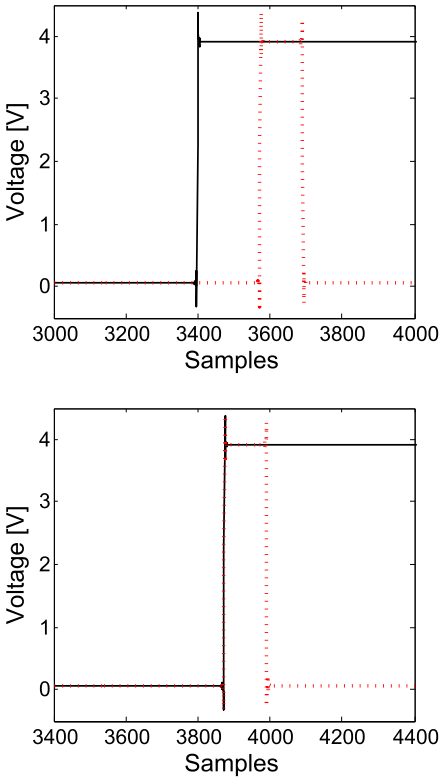

Fig. 7. The Continuous black line (long peak) represents the PPS signal and the dashed red line (shorter peaks) the periodic signal. Sampling frequency used for this test was 25 kHz. In the asynchronous mode (top plot), the sampling starts at a random time with respect to the PPS rising or falling edges. In the synchronous mode (bottom plot), the two peaks are synchronized.

1) Synchronization of the Sampling With the PPS: We synchronized the sampling clock on the PPS rising edge. The synchronization was tested with two different sampling rates, 15.625 and 25 kHz, for >94 h (340 786 s). The second rate is used to confirm that the synchronization is independent of the sampling rate. In both scenarios, the number of samples remains constant between pulses.

2) Test With GPS Signal Loss: In order to test the system behavior when TFP loses the GPS signal, we commuted the TFP from GPS mode to its fly mode (internal clock). We acquired 350 files with 500 data blocks each. The size of each block was 1024 samples at 25 kHz. We tested a GPS signal interruption lasting 47 min 47 s, which seems a possible scenario. The total test duration was $350 \times 500 \times 1024/25\,000 = 7168$ s and we counted exactly 7168 PPS within the data. All pulse intervals contained 25000 samples. Therefore, the TFP maintained the sampling synchronized with the PPS signal.

V. Timestamp

A modern board using an integrated PTP synchronization will provide a timestamp synchronized with the beginning of the DAQ. In our present case, when the acquisition starts, a timestamp (epoch since January 6, 1980) is requested from TFP, which is further written into the data file header. A small delay is introduced due to the TFP request/response processing time. We tested this processing time with the acquisition of 7200 files. It takes an average of 12 ms with a standard deviation of 4 ms (Fig. 8).

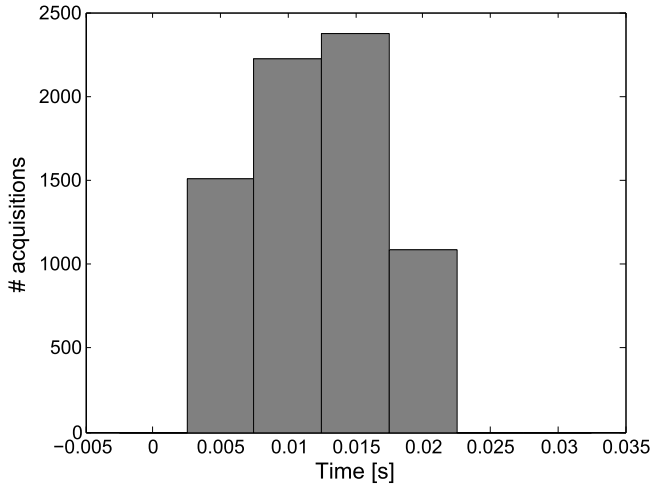

Fig. 8. Time delays to obtain the GPS timestamp from 7200 requests.

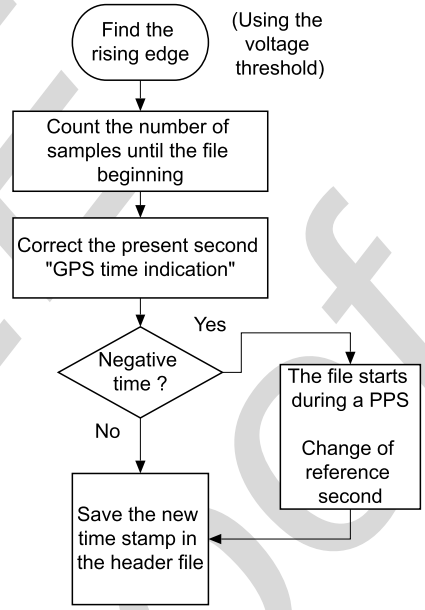

Fig. 9. Flow chart of the algorithm.

A. Finding the Acquisition Starting Time

The data are synchronized with the PPS signal as they are sampled simultaneously. In order to correct the acquisition starting time, we developed an algorithm, implemented in the SDAQ, that uses the PPS (Fig. 9). The procedure consists of two main steps.

The first step identifies the first complete PPS pulse based on its features. The PPS is a square signal with a 20% duty cycle (200 ms) [26], [27] with low and high levels of 0.1 and 3.9 V, respectively. It is possible to acquire a sample during the level switching within sampling rates between 15.625 and 50 kHz. Therefore, we estimated the level switching duration as $<2/50\,000$ s. The sampled voltage value taken during the rising and falling edges differ and they also depend on the sampling rate used. In the case of 15.625 kHz, the values are ∼3 and ∼1 V, as shown in Fig. 10. Respectively, for the rising and falling edges. These values are nearly constant and, therefore, we can fix a threshold ∼3.5 V. If two successive

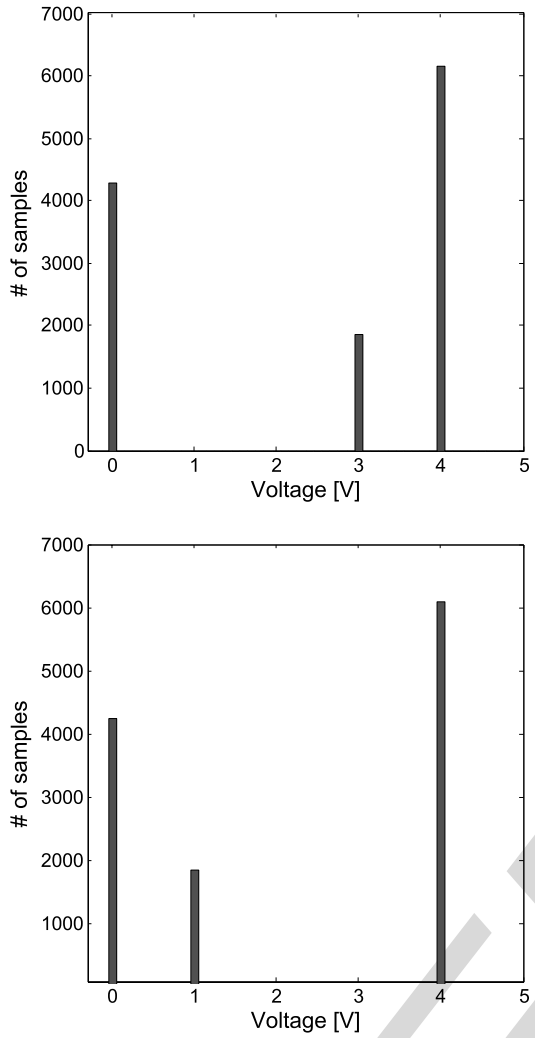

Fig. 10. Histogram of samples around the threshold value. Three peaks correspond to the low, the intermediate, and the high sample values of the rising edge (top plot) and the falling edge (bottom plot). Binning corresponds to 0.1 V and 12 000 PPS were tested. Sampling is 15.625 kHz.

samples are below and above this threshold, it is guaranteed that the edge is identified.

The second step consists in correcting the registered time. The time span between the first data point and the rising edge of the first complete PPS pulse is computed by counting the number of samples in between. The acquisition starts at any random time with respect to a PPS pulse; therefore, the GPS time can be read during an ongoing pulse or before a completed one. However, as shown in Fig. 8, the request/response processing time is much <1 s; therefore, using this information, we are able to identify the time second corresponding to the first complete PPS, and then correct the timestamp of the first data point.

This step is only possible after confirming that no data were lost (see Section III) and the number of samples between PPS pulses is constant (Section IV).

B. Controlling the Timestamp Correction

In order to confirm that the algorithm provides the correct timestamp, time intervals between starting times were tested from 7200 consecutive files. These time intervals were found to be constant, 4.096 s, indicating that timestamps are correctly given. The systematic error in this process is <1/fs.

C. Electronic Delay of the PPS Signals

In order to characterize the electronic delay, a second GPS receiver was connected to the ADC. Both PPS signals were acquired simultaneously at 50 kHz to check for possible mismatching. A comparison between the rising edge of 3071 PPS pulses from both GPS receivers was carried out. All edges were found in the corresponding samples. The electronic delay is, therefore, estimated to be $<1/50\,000 = 20$ μs, which is included in the systematic error.

VI. Conclusion

The last run of the Schenberg GW detector occurred in 2008. Since then the detector has been upgraded. However, the DAQ hardware used at that time could not be replaced due to budget restriction. The acquisition of a PTP or other protocol compatible hardware would require a complete change of the present VXI setup (ADC, TFP/GPS, and VXI-PC board).

We identified different problems within the present DAQ that could compromise the data timestamp reliability and, consequently, a possible GW confirmation. Therefore, we proceeded with a complete DAQ reconfiguration. The main problem, the data block loss, was solved by managing the ADC buffer and using different acquisition modes. Different options were tested to reduce the sampling rate irregularities. The final solution was to use TFP-PPS synchronization to drive the sampling. The sampling, in this configuration, is constant showing exactly the same number of samples between each PPS pulse.

This new configuration permits the use of samples as a reference to define the correct timestamp. As the low latency data analysis requires this to be done online, this definition is directly implemented into the DAQ software. Each PPS edge is a time reference of 1-μs precision, but as shown, the final time resolution is only limited by the sampling rate as needed. The systematic error is $\lesssim$1/fs and possible electronic delays are included in this timing error. The new timestamp has, therefore, a precision two orders below previous experiment of the same kind, 64 μs compared with $\sim$10 ms.

This solution perfectly fulfills our GW search needs. It has the advantage of being easily implemented in most common DAQ boards. Its timestamp reliability is equivalent to the use of a PTP compatible solution. The only counterpart is that the ADC has one less available channel as it is required to record the PPS signal.

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Timestamp Reliability of the Schenberg Gravitational Wave Detector Data Acquisition System

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***Abstract*— The Schenberg gravitational wave (GW) detector has been under development for the past few years. A scientific run is planned for the near future. The main technique used to confirm a GW is the search for time coincident events between multiple detectors. Therefore, a reliable timestamp is essential for events found in data from each detector. In the particular case of the Schenberg detector, we are planning a low latency analysis, which requires that no data sample be lost during either data acquisition (DAQ) or transmission, and that time correction be done online. The aim is to provide reliable data where each sample carries its own timestamp information. GW event candidates are pointed out after a dedicated analysis and their time of occurrence are determined by these samples. We present here the DAQ solution developed for the Schenberg detector. It is easy to implement this solution using equipment commonly found in most laboratories. No specific equipment using precision time protocol or other protocol was needed to synchronize the sampling. In addition, no transmission time is needed to be explicitly known. The timing precision is limited only by the chosen sampling frequency, which fulfills the data analysis needs.**

***Index Terms*— Astronomy, data acquisition (DAQ), detectors, synchronous detection, timing.**

I. Introduction

SCHENBERG is a gravitational wave (GW) detector, which uses a spherical resonant mass with a high mechanical quality factor $Q \sim 10^7$. The sphere's mass and diameter are 1150 kg and 65 cm, respectively, which leads to a resonant frequency $f_0 \sim 3.2$ kHz. GWs couple to the sphere's five quadrupolar modes [1], [2]. The sphere's mechanical oscillations are then converted into electromagnetic signals by six resonant transducers with klystron-type cavities [3]. A 10-GHz microwave signal is pumped into the resonant cavity and modulated by its oscillations ($df/dx \sim 0.5$ GHz/μm) [4], [5]. This signal is then demodulated, amplified, and digitized for subsequent analysis.

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Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

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A high precision timestamp and strict data continuity are two critical requirements for GW data analysis. The most common procedure to confirm GW detection is a coincidence blind search between multiple detectors. If coincident signals, above SNR ∼5, happen to be found in three detectors, in a typical time window of 1 s, the probability of a false positive would be $1/10^4$ year.[1] The time window depends on each detector's time resolution. Thus, the better the time resolution, the lower the false alarm rate is [6]–[9]. The previous resonant mass detectors NAUTILUS, EXPLORER, and Allegro provided a precision of 12.8, 6.4, and 8 ms, respectively [6], [10].

Previously, data timestamp corrections were performed during offline analysis. In the present case, we are aiming at a low latency analysis with a delay <1 s for 30 s of data [11]. Therefore, all corrections need to be executed online.

Another point is the search for periodic signals. In this kind of research, any sample lost or time shifted might be interpreted as a frequency shift or power loss of the source signal [12]–[14].

Protocols as network time protocol (NTP) [15], [16], precision time protocol (PTP) [17]–[19], and white rabbit (developed at CERN) [20], [21] allow the synchronization of clocks within a defined network in the respective ranges of ∼10 ms, sub-μs, and ns. In our case, a GPS receiver is already integrated in the data acquisition (DAQ) system and there is no need to propagate the synchronization to other systems.

These protocols are perfect to timestamp discrete events (considering electronic delays). For example, we keep a record of cosmic ray showers hitting the detector and use NTP to mark their timestamps [22].[2] In the case of potential GW signals, we need to perform many transformations (Fourier transform and its inverse, aliasing, filters, and others) on the data before timestamping a potential GW event. Therefore, it is easier for the GW analysis if each sample carries the timestamp information in the same way, for example, such as the one used in very long base interferometry [23], where the sampling is synchronized with integrated systems of high-frequency clocks and GPS. The GW detector

[1] The threshold SNR vary in function of the noise of each detector.

[2] The cosmic ray veto is presently connected to another DAQ system. The two DAQ evolve separately, their data are completely different.

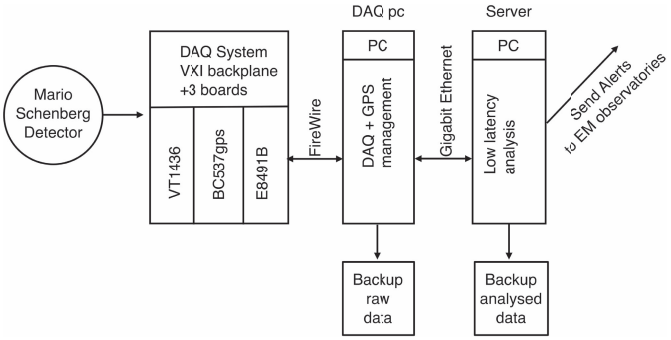

Fig. 1. Schematic of the DAQ setup. Analog-to-digital conversion is done by a VTI Instruments VT1436 board. Time reference is provided by a TFP BC537gps from symmetricom. Finally, the bridge between VXI backplane and DAQ PCs is performed by an Agilent board E8491B.

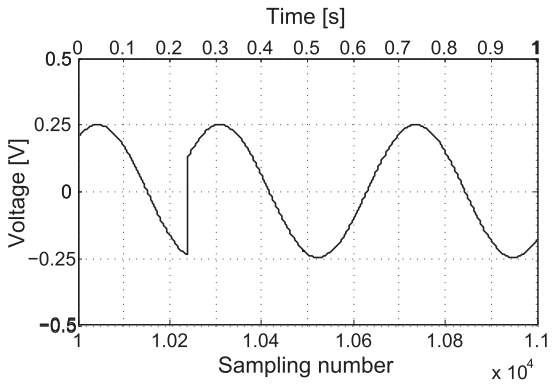

Fig. 2. Data loss due to the block mode. We used a signal generator with a sinusoid of 60 Hz to check the continuity of our DAQ. Sampling is 25 kHz.

LIGO has developed its own boards with high-frequency clocks (∼8.4 MHz) to provide synchronized sampling [24]. In our case, we can indeed use one of the above methods to timestamp our samples, principally the PTP. One approach is to use analog-to-digital converters (ADCs) based on the LXI standard (class B or C), which are compatible with PTP. However, we need to maintain a legacy VXI system, which is not compatible with this protocol. In addition, currently, there are only a few vendors providing analog-to-digital boards with timestamped data, as shown in the LXI product page [25].

Therefore, GW data analysis does not need a better time resolution than the one given by the sampling rate. Then, preserving the existent equipment, we present here a solution where the sampling is synchronized with a conventional time frequency processor (TFP) clock, which is itself synchronized with GPS pulse per second (PPS). The Schenberg detector DAQ setup (ADC, TFP/GPS, and VXI-PC board) is described in Section II. It is configured to provide a data stream without any interruption.

In previous measurements, we encountered technical problems that appeared as data loss. This problem, along with its solution, is described in Section III. Once we ensured data continuity, we synchronized the sampling with GPS PPS (Section IV). To conclude this method, a technique to retrieve the timestamp using PPS signal recorded by the ADC is described in Section V.

II. DAQ Setup

The Schenberg DAQ system is based on a VXI CT-400 backplane, as shown in Fig. 1. The CT-400 chassis has 13 slots, where three of them contain the boards (C-size industry standard).

Time reference is provided by an Symmetricom TFP BC537gps. It uses an external GPS to provide the time with a precision of 1 μs. In case of GPS signal loss, its internal clock assumes the relay. During DAQ, we record an extra channel containing its PPS signal. As shown below, the TFP also drives the ADC external trigger.

Transducer signals are digitized by an ADC VT1436 board from VTI Instruments. It provides 16 channels with a maximum sampling of 102.4 kSa/s and a DRAM memory buffer of 32 MB (16 MSa) divided by the number of channels. Each sample is 2-B long. Seven channels are used for the transducer signals and one for the PPS signal. The remaining channels will be used for auxiliary sensors (i.e., seismometers, magnetometers, and voltmeters).

The interface between VXI backplane and DAQ PCs is performed by an Agilent board E8491B. The data are transferred via industry standard IEEE-1394 bus (firewire, 400 Mb/s).

One PC is fully dedicated to DAQ, whereas another PC is used as a server and to perform the real-time analysis. The low latency pipeline accesses the data stream generated by the DAQ software. The data are transferred for analysis with their own timestamps.

A. DAQ Software

Using MATLAB, a software, named SDAQ, with a graphical user interface to manage the DAQ was written.[3] It allows the user to set parameters, such as channel selection, sampling rate, voltage range and data block size, and displays the acquisition status. It also provides two online data displays: 1) spectrum analyzer and 2) oscilloscope.

When starting the DAQ, the program automatically configures the TFP and the ADC with predefined parameters.

III. Continuity of the Data

The ADC works on a first in, first out principle. The transmission from the ADC buffer to the PC is performed by sending data blocks of different possible sizes, such as 1024, 2048, and 4096 samples. It is possible to transfer these blocks using two different modes.

In the block acquisition mode, the system waits until the data are transferred before continuing the acquisition. If the command that asks for the data transfer is delayed, data blocks are not collected during this period, and are, therefore, lost, as shown in Fig. 2. There are different reasons why this delay can happen, but it is mainly due to the time lag when sending the request of a new block synchronously with the acquisition.

In the continuous acquisition mode, the data are continuously acquired independently of the transfer command.

[3]LabView could be seen as a better environment to develop a DAQ program, but our choice was due to logistic and practical reasons.

TABLE I
MAIN PARAMETERS OF THE TWO TESTED SIGNALS

Signal	Sine (100 Hz)	Ramp (5 s)
Sampling [kHz]	25	25
Block size [samples]	1024	1024
Number of blocks per file	500	500
Number of files	2110	2110
Number of PPS	43213	43213
Total time [s]	43212,8	43212,8

This mode avoids the previous problem, but it has two issues depending on the number of data blocks to be transferred. If the chosen number of data blocks is too small, the blocks will be ready before the software sends the request to acquire them. After a while, the buffer capacity will be exceeded and data are lost. If the number of blocks is excessive, we can also overload the buffer.

The data transfer from the ADC board to the DAQ PC takes 17.3 ± 4.5 ms. Therefore, the DAQ time should be longer than this. Therefore, we round the transfer time to 22×10^{-3} s and the minimum number of samples is given by

$$\mathrm{NS}_{\min} = 22 \times 10^{-3} \cdot f_s \tag{1}$$

where NS is the number of samples and f_s is the sampling frequency [Hz]. Then, the minimum number of blocks NB is given by

$$\mathrm{NB}_{\min} = \frac{22 \times 10^{-3} \cdot f_s}{\mathrm{bs}} \tag{2}$$

where bs is the block size. The maximum number of blocks is

$$\mathrm{NB}_{\max} = \frac{16 \times 10^{6}}{8\mathrm{bs}} \tag{3}$$

where we considered eight channels and 16×10^6 is the buffer size in sample number. The DAQ sampling rate is $f_s = 15\,625$ Hz, which implies, using a block size of 1024 samples, that the minimum number of blocks is 1 and the maximum number is 1953.

A. Testing the Continuity

We tested the DAQ continuity by measuring two different signals. First, we applied a low-frequency ramp signal with a period of 5 s. Then, we measured a sinusoidal signal with a frequency of 100 Hz. Both signal amplitudes were 5 V peak-to-peak. In both the cases, the PPS signal was recorded at the same time. In Table I, we report the main parameters of these two tests with the number of PPS measured.

1) Test Using a Ramp Signal: This test serves to check the software management of acquisition. If there is a discontinuity, it should happen between block transfer and, therefore, be shown as steps on the ramp. No such feature was observed.

2) Test Using a Sinusoidal Signal: We recorded 2110 files containing 500 data blocks of 1024 samples, equivalent of ~12 h, with a continuous 100-Hz sinusoidal signal. We used a higher sampling frequency (25 kHz) instead of 15 625 Hz to stress the system. With a higher sampling frequency, the data loss conditions (overload) mentioned above is reached faster.

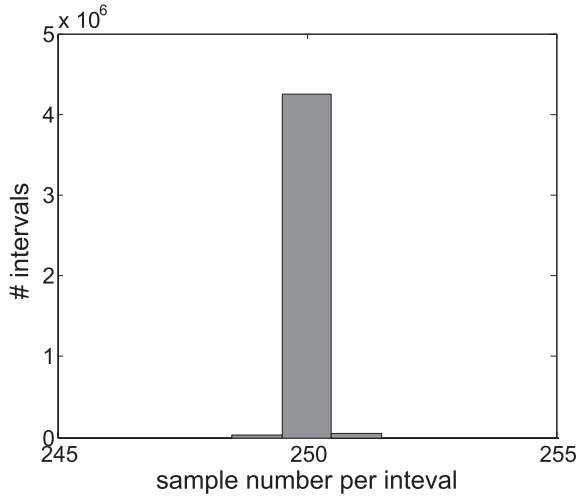

Fig. 3. Number of bins per period. Sampling is 25 kHz and the signal frequency is 100 Hz.

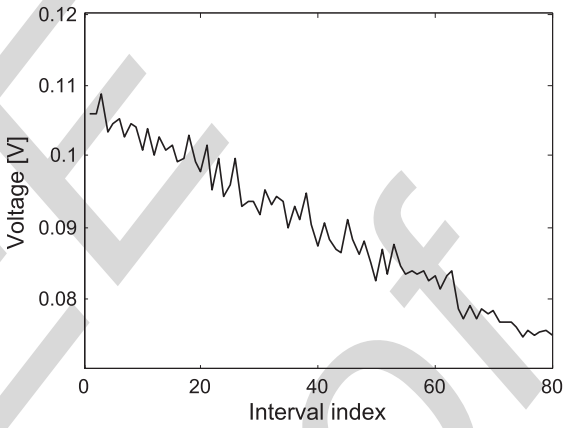

Fig. 4. Value of the first samples of 80 periods.

In Fig. 3, we report the measured number of samples per period, which should be sampling/signal frequency = 25 000/100 = 250. The total expected sample number is 1 080 320 000. We measured $4\,249\,024 \times 250$ samples, $29\,100 \times 249$ samples and 43100×251 samples, which gives a total of 1 080 320 000 samples. No data were lost.

In order to understand the number of sample deviation, we performed a fast Fourier transform of the signal over 211 files and got a frequency of 99.9986 Hz and, therefore, the period is 250.0035 samples. This value is confirmed by dividing the number of data by the number of periods that we obtain, the period lasts 250.003 samples. We also tested the first nonzero value of 80 consecutive sine periods (Fig. 4). There is a slight decrease in these values at every 250th sample, which means that each time the signal period is starting earlier than the previous period and thus the signal period is >250 samples. Actually, we will see below that the sampling rate is also not regular. This irregularity can also contribute to this variation.

IV. SAMPLING REGULARITY

In order to use the number of samples and PPS to provide timestamps, the sampling rate should be constant between pulses.

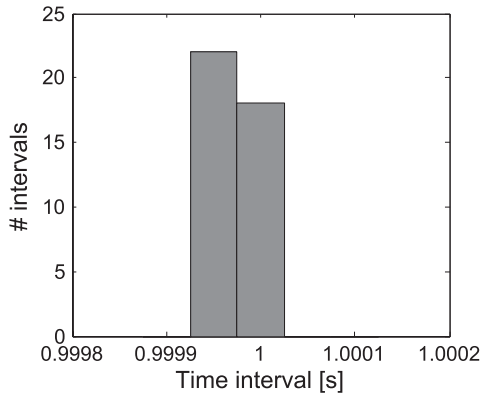

Fig. 5. Histogram of 40 pulse intervals obtained from a 40 s acquisition. Each bin represents 39 μs.

The ADC VT1436 can either use its internal clock or an external one to generate sampling frequencies. The range of available internal clock frequencies is from 40.96 to 102.4 kHz. In both the cases (internal or external clocks), sampling frequencies are defined as the set clock frequency divided by 2.56. From these primary sampling frequencies, the ADC generates other ones by dividing them either by 5 or by powers of 2 or by both.

We noticed that when the internal clock was used, the ADC sampling rate was not constant between two consecutive pulses. For example, we set the sampling rate to 25 kHz and counted the number of samples between pulses.[4] The result of 40 s of acquisition is shown in Fig. 5. Around half of the pulse intervals had smaller sample counts than the expected 25 000. After 24 h, the accumulated delay was ~1.7 s. This is an excessive shift for the analysis, remembering that the coincidence search is typically performed within a 1 s window. Therefore, the number of samples could not be used as a marker to count time intervals.

A. Using TFP Clock to Drive ADC Clock

Since the GPS receiver has a 1-μs precision, which is smaller than the sampling rate, we use the TFP internal clock to drive the ADC sampling.

1) Connecting the TFP BC537gps and the ADC VT1436: The average measured voltage of the TFP BC537gps clock are ~3.9 and ~0.1 V, at the highest and lowest levels, respectively, which are transistor–transistor logic compatible as required by the ADC VT1436. Therefore, neither amplification nor attenuation was needed. All tests described below were performed using this signal.

We used the external sample SubMiniature version B connector (SMB) connector on the ADC front panel to connect the external clock. The TFP output is a 15 pin D socket. Therefore, we built a 15 pin D plug to SMB adapter, which connects both boards (Fig. 6). This adapter actually carries both signals: 1) the PPS and 2) the external clock.

The TFP driving clock can be programmed to fit the ADC range by the following expression: 1) $f_{\text{clk}} = 10\ \text{MHz}/(n_1 \times n_2)$, where 10 MHz is the TFP BC537gps internal clock and 2) n_1 and n_2 are two programmable values. For example, to achieve 100 kHz, $n_1 = 2$ and $n_2 = 50$. The clock frequency generated by the TFP is chosen to match an internal ADC one to avoid radical changes in the sampling rate in the case of a system failure. If the ADC loses the external clock, it will use the closest internal sampling frequency available. The frequencies generated by the TFP that match the ADC VT1436 internal frequencies, and which are between the admissible range (40.96–102.4 kHz), are: 50, 62.5, 78.125, 80, and 100 kHz.

[4]The number of samples was also tested with many others sampling frequencies. In all cases we found a deviation in the number of samples between pulses.

Fig. 6. Picture showing the three boards. BC537gps is located in the middle where one can see the 15 pin D plug with two cables (PPS and the external clock signals) leaving it. Just above it, the cable to the GPS antenna can be seen. VT1436 board is on the right and the E8491B board is on the left.

The Schenberg resonant frequency is ~3.2 kHz and, therefore, the sampling rates need to be >6.4 kHz. Considering the external and internal clock compatibility and the sampling constrains, we have implemented the following list of sampling frequencies, such as 10, 12.5, 15.625, and 20 kHz. For our measurements, we are using 15.625 kHz. This choice is justified by a compromise between an improved time resolution, 64 μs, with respect to previous experiments (~10 ms) and to avoid an excess production of unnecessary data, which will slow down the analysis.

2) TFP Periodic Signal and PPS Signal Synchronization: The clock signal generated by the TFP can be synchronous or asynchronous with the PPS, as shown in Fig. 7. In order to control the number of samples between pulses, we use the synchronous mode.

B. Testing the Sampling Regularity

After having connected the two boards, we executed the following two tests.

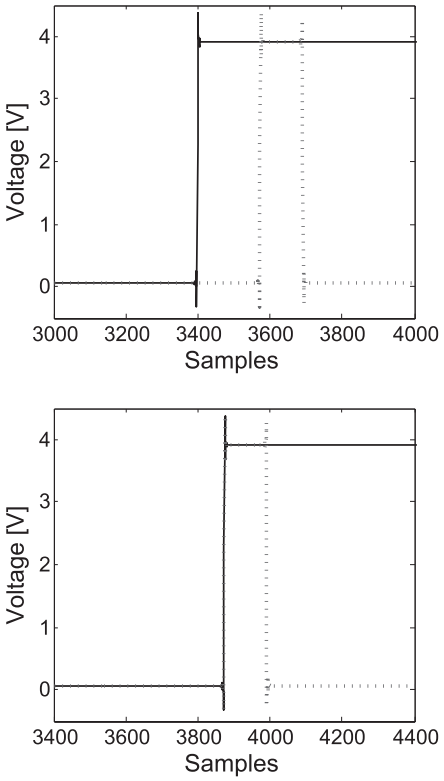

Fig. 7. The Continuous black line (long peak) represents the PPS signal and the dashed red line (shorter peaks) the periodic signal. Sampling frequency used for this test was 25 kHz. In the asynchronous mode (top plot), the sampling starts at a random time with respect to the PPS rising or falling edges. In the synchronous mode (bottom plot), the two peaks are synchronized.

1) Synchronization of the Sampling With the PPS: We synchronized the sampling clock on the PPS rising edge. The synchronization was tested with two different sampling rates, 15.625 and 25 kHz, for >94 h (340 786 s). The second rate is used to confirm that the synchronization is independent of the sampling rate. In both scenarios, the number of samples remains constant between pulses.

2) Test With GPS Signal Loss: In order to test the system behavior when TFP loses the GPS signal, we commuted the TFP from GPS mode to its fly mode (internal clock). We acquired 350 files with 500 data blocks each. The size of each block was 1024 samples at 25 kHz. We tested a GPS signal interruption lasting 47 min 47 s, which seems a possible scenario. The total test duration was $350 \times 500 \times 1024/25\,000 = 7168$ s and we counted exactly 7168 PPS within the data. All pulse intervals contained 25000 samples. Therefore, the TFP maintained the sampling synchronized with the PPS signal.

V. Timestamp

A modern board using an integrated PTP synchronization will provide a timestamp synchronized with the beginning of the DAQ. In our present case, when the acquisition starts, a timestamp (epoch since January 6, 1980) is requested from TFP, which is further written into the data file header. A small delay is introduced due to the TFP request/response processing time. We tested this processing time with the acquisition of 7200 files. It takes an average of 12 ms with a standard deviation of 4 ms (Fig. 8).

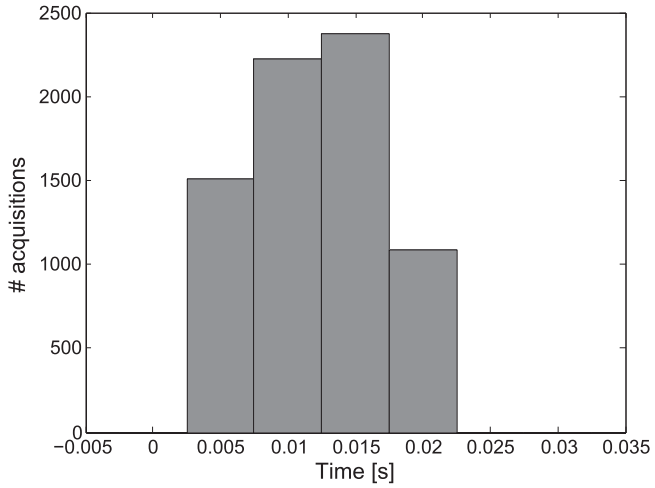

Fig. 8. Time delays to obtain the GPS timestamp from 7200 requests.

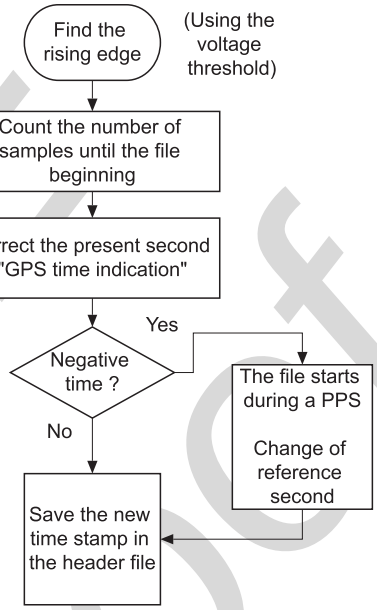

Fig. 9. Flow chart of the algorithm.

A. Finding the Acquisition Starting Time

The data are synchronized with the PPS signal as they are sampled simultaneously. In order to correct the acquisition starting time, we developed an algorithm, implemented in the SDAQ, that uses the PPS (Fig. 9). The procedure consists of two main steps.

The first step identifies the first complete PPS pulse based on its features. The PPS is a square signal with a 20% duty cycle (200 ms) [26], [27] with low and high levels of 0.1 and 3.9 V, respectively. It is possible to acquire a sample during the level switching within sampling rates between 15.625 and 50 kHz. Therefore, we estimated the level switching duration as $<2/50\,000$ s. The sampled voltage value taken during the rising and falling edges differ and they also depend on the sampling rate used. In the case of 15.625 kHz, the values are ∼3 and ∼1 V, as shown in Fig. 10. Respectively, for the rising and falling edges. These values are nearly constant and, therefore, we can fix a threshold ∼3.5 V. If two successive

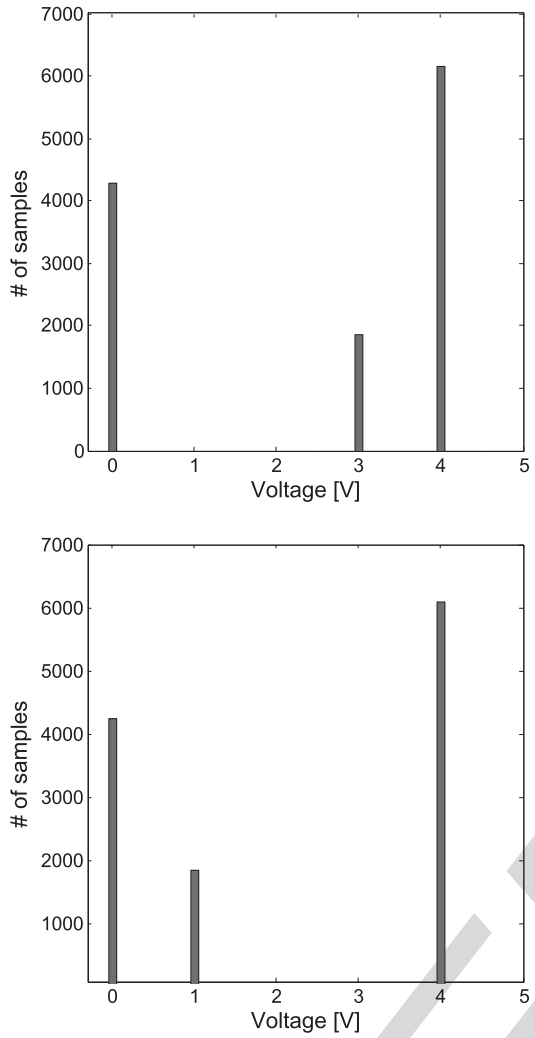

Fig. 10. Histogram of samples around the threshold value. Three peaks correspond to the low, the intermediate, and the high sample values of the rising edge (top plot) and the falling edge (bottom plot). Binning corresponds to 0.1 V and 12 000 PPS were tested. Sampling is 15.625 kHz.

samples are below and above this threshold, it is guaranteed that the edge is identified.

The second step consists in correcting the registered time. The time span between the first data point and the rising edge of the first complete PPS pulse is computed by counting the number of samples in between. The acquisition starts at any random time with respect to a PPS pulse; therefore, the GPS time can be read during an ongoing pulse or before a completed one. However, as shown in Fig. 8, the request/response processing time is much <1 s; therefore, using this information, we are able to identify the time second corresponding to the first complete PPS, and then correct the timestamp of the first data point.

This step is only possible after confirming that no data were lost (see Section III) and the number of samples between PPS pulses is constant (Section IV).

B. Controlling the Timestamp Correction

In order to confirm that the algorithm provides the correct timestamp, time intervals between starting times were tested from 7200 consecutive files. These time intervals were found to be constant, 4.096 s, indicating that timestamps are correctly given. The systematic error in this process is <1/fs.

C. Electronic Delay of the PPS Signals

In order to characterize the electronic delay, a second GPS receiver was connected to the ADC. Both PPS signals were acquired simultaneously at 50 kHz to check for possible mismatching. A comparison between the rising edge of 3071 PPS pulses from both GPS receivers was carried out. All edges were found in the corresponding samples. The electronic delay is, therefore, estimated to be $<1/50\,000 = 20$ μs, which is included in the systematic error.

VI. Conclusion

The last run of the Schenberg GW detector occurred in 2008. Since then the detector has been upgraded. However, the DAQ hardware used at that time could not be replaced due to budget restriction. The acquisition of a PTP or other protocol compatible hardware would require a complete change of the present VXI setup (ADC, TFP/GPS, and VXI-PC board).

We identified different problems within the present DAQ that could compromise the data timestamp reliability and, consequently, a possible GW confirmation. Therefore, we proceeded with a complete DAQ reconfiguration. The main problem, the data block loss, was solved by managing the ADC buffer and using different acquisition modes. Different options were tested to reduce the sampling rate irregularities. The final solution was to use TFP-PPS synchronization to drive the sampling. The sampling, in this configuration, is constant showing exactly the same number of samples between each PPS pulse.

This new configuration permits the use of samples as a reference to define the correct timestamp. As the low latency data analysis requires this to be done online, this definition is directly implemented into the DAQ software. Each PPS edge is a time reference of 1-μs precision, but as shown, the final time resolution is only limited by the sampling rate as needed. The systematic error is $\lesssim$1/fs and possible electronic delays are included in this timing error. The new timestamp has, therefore, a precision two orders below previous experiment of the same kind, 64 μs compared with $\sim$10 ms.

This solution perfectly fulfills our GW search needs. It has the advantage of being easily implemented in most common DAQ boards. Its timestamp reliability is equivalent to the use of a PTP compatible solution. The only counterpart is that the ADC has one less available channel as it is required to record the PPS signal.

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